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Applying Materials in the Perfect Storm

Brace for the three-front tech storm: a shift to big 300 mm wafers, fantastically smaller lines, and new deposition tools and materials

Jim Morgan's law: The number of transistors on a wafer doubles even faster than you think. Gordon Moore's 18-month doubling rate refers to transistor density—the number of transistors per square inch of silicon wafer. But wafers grow too: 50 millimeters (mm) in diameter in 1970, 200 mm a couple of years ago. Intel's (INTC) first 300 mm fab went on line in early '02, and 450 mm wafers are now on the horizon. To understand both the meteoric growth of information technology and the boom-bust character of that growth, look first to Morgan's law, not Moore's.

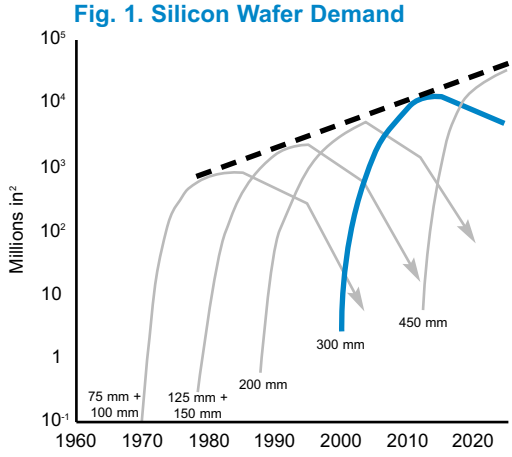
We'll get back to Jim Morgan in a moment, but first things first. The world builds logic structures on almost 5 billion square inches—about 800 acres, or just over one square mile—of silicon every year. The silicon itself emerges from foundries that purify and crystallize semiconductor materials (*Quantum Foundry*, January 2003)—these foundries are the 21st century's steel mills. Machine tools then transform the raw crystals into functional structures—a square inch of semiconductor becomes about $25 (on average) of value product—hence the $120-billion global market for integrated circuits.

No serious student of our modern economy can doubt that the 5-billion square inches will become 10, and then 20, and then 100, or that the $120 billion will grow to $250 billion, and then to $1 trillion. For most of human history, humanity fought for land because land supplied crops and trees, and thus bulk material and energy, which are the essential starting points in the pursuit of everything else. The Industrial Revolution changed that picture only in that the struggle came to center more on resources buried beneath the land, particularly coal and oil. That era is now fading into history. The essential real estate is measured today by the square inch, not by the square mile. The square mile of semiconductors the world produces every year supplies more wealth, more power, and more global dominion than entire continents' worth of arable land.

The value extracted from the silicon real estate doesn't come from peasants who till the soil, nor even from workers who labor tirelessly in the din of the factory floor. It comes from machines. The first thing you notice when you walk into a chip fab is that you don't walk into a chip fab. Almost no one does. What you walk up to, if you even get that close, is a hermetic viewing window. On the other side, you may or may not see a couple of people in bunny suits. Mainly, however, what you see is tens of millions of dollars of immaculate equipment. This is what Henry Ford's assembly line has come to, and what the foolish Karl Marx most feared: a factory in which capital has almost wholly displaced labor. The machines do what the hand weavers did before the automated loom—for all practical purposes, they do everything. The handful of workers in the chip fab don't manufacture chips; they mind the chip-manufacturing machines.

There are about 900 chip fabs worldwide. Each one costs $1 to $2 billion to build and equip. The machines and tools—not the land, labor, buildings, or raw materials—account for the lion's share of that cost. Some of the machines provide extremely pure water, air, and chemicals. Others provide extremely stable electricity. Still others assemble, package, inspect, and test the chips—this group comprises the second largest share of overall fab capital spending, accounting for about $7 billion a year, globally. The rest—which account for over two-thirds of the semi equipment business, or about $17 billion in annual spending—perform one of three fundamental functions: They deposit material on a surface (grow, dope, implant, and heat-treat); they paint blueprints on the surface so-formed (photolithography); or they

Fig. 1. Silicon Wafer Demand



Source: "Limits of Integrated Circuit Manufacturing," Doering, *Proceedings of the IEEE* (March 2001).

remove material from the surface as dictated by the blueprint (etching, polishing).

Which brings us to Applied Materials (AMAT) and its CEO, Jim Morgan. Applied Materials builds the high-precision tools that shape, form, and join semiconductors in the manufacture of logic chips, powerchips, and electron-to-photon conversion devices. Morgan is one of a handful of early CEOs of a major Silicon Valley tech company who, unlike all the rest, remains CEO today. Applied's machines—as the company itself often points out—are involved in the manufacture of nearly every microchip on the planet. They will be for years to come. Among the manufacturers of the tools that manufacture the chips, no other company ranks in the same league.

The memories of the tech bubble and its collapse may still be too fresh and bitter for many investors to feel confident about putting their money back into anything associated with semiconductors. But now is the time to take a close look at the underlying digitally powered, material-moving machines that manufacture integrated circuits and that account for the sharply cyclic fortunes of this extraordinary industry. We believe the industry is on the threshold of the next huge upswing, and we'll tell you why. Even if we're wrong about some of the details, global semiconductor output will continue to double and redouble every few years for as long as we live. It's almost impossible to imagine how the leading manufacturer of the essential manufacturing tools of the post-industrial economy could, over the longer term, fail to prosper.

Wavelengths, Wafers, and Wells

The prime movers of the information age are the photolithographers—the artists of light. Photolithography prints an ultra-fine photograph of a desired pattern by selectively removing a chemical that coats the surface of a wafer. The wafer is then exposed to an etching chemical that eats away material only where the coating has been removed, leaving behind elevated structures where the coating remains in place. The coating on the roofs of those structures is then washed off, and a new material layer is deposited, another pattern is printed, there's another round of etching, and cleaning. In this manner, through hundreds of successive steps, elaborate, three-dimensional structures are erected, floor by floor, in the same manner as skyscrapers, on the wafer's surface. Pushed to its current limits, this fantastically complex and delicate process can build a city with 50 million microscopic buildings, linked together by kilometers of interconnecting wires, on a surface about the size of a postage stamp.

Moore's law reflects, first and foremost, the ever-improving quality of our optics. How microscopically small the structures of an integrated circuit can be depends, in the first instance, on the optical resolution of the ultra-specialized, pattern-conveying "laser printers." Twenty years ago, the photolithographers were using bright lamps, then they progressed to "soft" ultraviolet light and then to ever shorter UV wavelengths, and in due course, they'll move into the X-ray bands. Lasers have replaced lamps, providing light much less prone to dispersion. Current technology uses the 248 nanometers (nm) light from krypton fluoride excimer laser to print 130 nm lines, and 193 nm light from argon fluoride excimer lasers to print 110 nm lines. The next target is 70 nm lines, which will be printed with 157 nm light from fluorine excimer lasers. Early last year, a TRW (now Northrop Grumman (NOC)) subsidiary (Cutting Edge Optronics), working in collaboration with Sandia National Labs, demonstrated lithography using a "Plasma Extreme Ultraviolet" light source—a 13.4 nm light that will ultimately permit feature sizes below 30 nm. The Pentium 4 on your desktop today has 130 nm architecture.

Each reduction in wavelength lets you build smaller structures—smaller quantum wells, and thus smaller transistors, thinner insulating layers, and thus

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smaller capacitors and resistors, and thinner conducting wires. Shorter wavelengths thus lead to finer structures, and thus to, (1) more structures per unit area (Moore's law) and, (2) faster devices, because size determines how fast circuits can run. And that's about all there is to the story, at least according to most of the standard accounts of why the digital power from the desktop and PDA to the guided missile keeps doubling every few years.

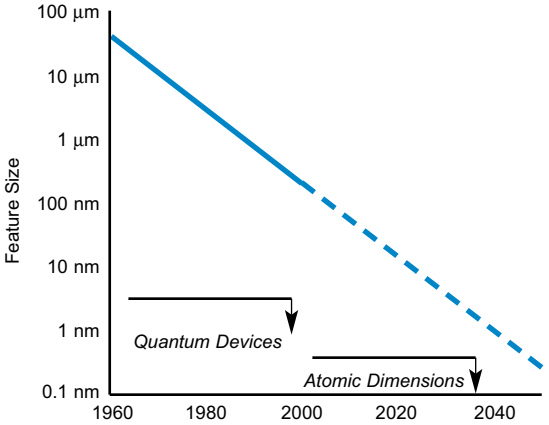
But patterns, however fine, are only the starting point: they have to be printed on to scaffolds—silicon wafers. For every $1 spent on lithographic tools, a chip fab invests at least $10 on all the equipment needed to translate the blueprints into solid, functioning material structures. And it is at this stage that three additional imperatives come into play. Two are essentially mechanical, the third is electrical.

To build a structure on a wafer, you add material. Heretofore, the two main processes used to add it have been chemical vapor deposition (CVD) and physical vapor deposition (PVD). CVD tools (used to deposit insulators and conductors, as well as semiconductors) direct gases containing the chemically reactive compounds at the wafer surface; these tools can process relatively large surface areas, but they run very hot (1000°C), which ultimately limits how finely you can build. Physical vapor deposition has the advantage of running at lower temperatures (500°C), but the price paid is somewhat poorer adhesion to the target surface. Both processes are fantastically delicate and precise compared to anything known to the world of practical engineering a decade or two ago—both will continue to evolve and play major roles in fabs. But both are nevertheless too blunt and crude to build structures smaller than about 100 nm.

To build most of the structures that fine, a remarkable new process has recently been commercialized—atomic layer deposition (ALD). ALD deposits atoms literally one layer at a time. By building up such layers, ALD can create material that conforms nearly perfectly to the scaffold beneath, covering corners (or steps) as immaculately as icing on a perfectly frosted cake. Importantly, ALD also happens at relatively low temperatures, which limits contamination. Its main disadvantages, until now, have been low speed and the difficulty of keeping an ALD process uniform across large wafers, and from wafer to wafer.

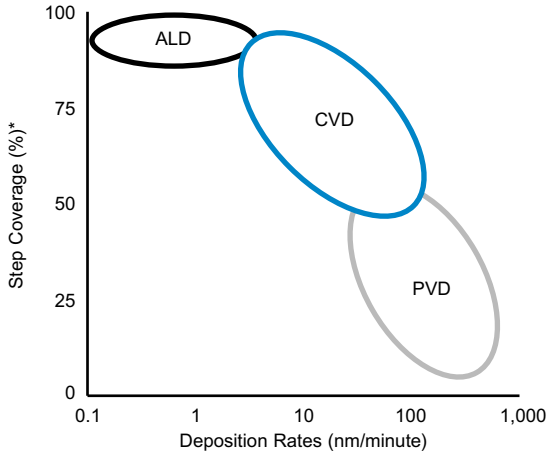
Even as the icing grows thinner, the cakes grow bigger. This is the second, fundamental, mechanical imperative in the chip-fab tool business. Chip fabs are step-by-step, batch-processing lines. Batches of wafers, each one a scaffold for batches of complete devices (e.g., entire CPUs), are put through one process, then

Fig. 2. Minimum Silicon Dimensions



Source: "Materials and Process Limits in Silicon VLSI Technology," Plummer, James D. and Peter B. Griffin, *Proceedings of the IEEE* (March 2001).

Fig. 3. Precision Deposition Technologies



** Share of sub-micron "steps" that are fully covered with deposited material.*

Source: "ALD Special Report: Where's the Metal?" Doe, Paula and Debra Vogler, *Solid State Technology* (January 2003).

cleaned, then put through another process, and so forth—several hundred steps in all to make a Pentium. The start-and-stop character of the process means that it is far cheaper to use larger wafers to build more devices. The hundred-dollar microprocessors that ran desktop PCs in the early 1980s cost only pennies today (and show up as embedded "microcontrollers" in appliances, machines, and toys) because much smaller lines and larger wafers now allow tens of thousands of these devices to be built simultaneously on a single wafer.

The move to larger wafers is not, however, a smooth or continuous process. Increasing wafer size requires a complete retooling of the fab—it's roughly equivalent to changing a Detroit assembly line from one that builds subcompacts, to one that builds SUVs, and then to one that builds large mining trucks—the platforms get big-

ger even while the component parts get smaller. In the fabs, those convulsive shifts happen about every eight years. Each one entails (roughly) a doubling in wafer area (a 50 percent increase in wafer diameter). And each requires massive new investment in capital equipment. The spending happens regardless, because it yields even greater economies—per-device manufacturing costs typically fall by (roughly) a factor of four.

The third, fundamental, engineering imperative is electrical, and it has come into play only quite recently. At some point, smaller structures require new materials—new conductors and new insulators. Chip engineers have, until now, been able to push the electrical performance of silicon, silicon oxides, and aluminum down to the current 130 nm state-of-the-art. But the aluminum and the silicon oxide are now reaching their limits.

All other things being equal, chip manufacturers would much prefer to build aluminum wires on their chips rather than copper ones, because aluminum is far less toxic to the surrounding semiconductor. But aluminum is a much worse conductor than copper, and when the chip-level wire diameters fall below about 100 nm, aluminum just can't handle the current. A few years ago IBM (IBM) and Motorola (MOT) pioneered a clever technique for building copper interconnections in ways compatible with the surrounding semiconductor chemistry. Implementing that process in a fab, however, requires an entirely new class of tools. It is a change at least as fundamental as, say, switching from wood to steel, or from steel to plastic, in a conventional factory. To implement changes that big, you don't "upgrade" an existing factory, you pretty much have to build a new one.

Insulators—"dielectrics"—present an equally big challenge, and, again, one that has only recently come to a head. Existing insulators—silicon dioxide, mainly—can still (barely) handle the 2 to 3 GHz speeds that CPUs now attain. But as structures get smaller they run faster, and when transistors start switching faster than about 5 GHz (20 GHz chips are now in early phases of design), the inherent capacitance of insulated wires becomes a serious problem—the insulators then begin imposing a speed limit on the entire device. The performance of silicon-dioxide insulators becomes unacceptable around about 100 nm lines. Some manufacturers have already started adding fluorine to the silicon dioxide to form fluorosilicate glass; that improves things a bit, but still not enough for structures under about 90 nm, and completely unacceptable when lines (inevitably) drop below 50 nm. Below 100 nm you have to go to carbon-doped oxides, or polymer-based insulators, and perhaps aerogel-like materials. Which requires, yet again, a major shift to entirely new tools.

These same material trends extend to logic's sister business, the $25-billion market for memory chips. Next-generation, smaller, faster, lower-power memory, both dynamic memory (DRAM) and "flash" (the billions of ubiquitous nonvolatile memory chips in PCs, cars, cell phones, and cameras), will use entirely new classes of materials: lead-zirconium-titanate (ferroelectric RAM), nickel, iron, and cobalt compounds (magnetoresistive RAM), or even selenium or tellurium compounds ("Ovonic" RAM).

The Perfect Storm

Weather forecasters witness a "perfect storm" only once every few decades, when three strong weather fronts converge at a single point. The first perfect storm of the chip manufacturing industry is now forming.

The industry has, of course, seen storms come and go before. Retooling is inherently episodic. Tools are extremely expensive, which encourages delays in retooling, particularly when economic times are tough. But once a critical mass of competitors takes the retooling plunge, all the rest of the industry has to race to catch up.

But this time around, things are different. Until now the photolithographers could deliver their improvements fairly incrementally, improving their techniques year-by-year to deliver finer and finer masks. But the masks have now grown so fine that they require completely new deposition tools—new ALD tools, for example, to replace the CVD and PVD tools that have served so admirably heretofore.

At the same time, the tool-makers are now delivering tools that can handle the pizza-sized 300 mm wafers. Infineon Technologies (IFX) was the first chip maker to build a 300 mm facility (for 64 megabit DRAMs) in Dresden, Germany, three years ago. A year ago, Intel began shipping production microprocessors built at their new 300 mm fab in Oregon, also the industry's first 130 nm production line on 300 mm wafers. The combination allows Intel to build about four times more processors per wafer than is possible with 180 nm on 200 mm wafers.

And finally, new tools are required to handle the new conductors and insulators without which the new, ultrafine logic structures cannot operate.

Any one of these shifts—new materials, new deposition processes, or larger wafers—would have propelled significant new investment in chip-fab tools. Taken together, they foreshadow a complete retooling of chip fabs around the globe. It will cost about $3 billion to build a new 300 mm wafer fab, compared to roughly $1.8 billion for the current 200 mm facilities. No chip manufacturer can view such investments as optional,

however; the question for all of them is not if, but when. Finer lines deliver at least five-fold improvements in performance, and larger wafers a four-fold reduction in cost. If your competitor buys into these new technologies, you will have to as well, or you'll be driven out of business. Stretching an extra few years of useful life out of yesterday's tools has merits, but is not a competitively viable option for the longer term.

Applied Materials

With $5 billion a year in sales Applied Materials is, by a wide margin, the world's dominant manufacturer of chip-fab tools. (See table.) Applied doesn't build photolithography tools, but it does build some tools used by the companies that build photolithography tools—the technology has advanced so far that it takes exotic tools to build the exotic tools. And photolithography aside, Applied builds most of the rest of the constellation of extraordinarily high-tech tools that do the construction work in every chip fab.

Last year, for example, Applied launched its Endura Integrated Copper Barrier/Seed (ICuBS) tool to deliver ALD capabilities to commercial chip fabs. The tool combines a plasma-vapor-deposition (PVD) chamber with an atomic-layer-deposition (ALD) chamber to allow the deposition of both tantalum nitride (TaN) to serve as a threshold barrier and bonding agent, followed by the copper to provide the electrical connections. Applied's tool can build the minuscule 1.5 nm films fast enough to meet current fab requirements. The ALD tool business is still small (under $100 million last year), with most of the tools still going into development labs, not manufacturing lines. But their pathway to the fab floor is now clear; total sales of ALD tools are forecast to exceed $1 billion in five years.

Applied's new "Black Diamond" tool is the first step in a march toward new dielectric materials. Using CVD technology, Black Diamond places carbon molecules as filler in the dielectric oxide. Adding carbon degrades the mechanical properties of the oxide, making the insulating layers more susceptible to the thermal and chemical stresses in subsequent stages of wafer processing. Applied has tuned the recipe to the point where Motorola has committed to launch a 130 nm chip using the Black Diamond tool and has a Black Diamond II in its roadmap for 90 nm devices. Competitors like Novellus (NVLS) and Dow (DOW) are pursuing a liquid spin-on process using a polymer that deposits as a porous layer which, in principal, can lead to even lower capacitance. But the spin-on process tends to absorb unwanted contaminants in subsequent processing, requiring yet-to-be-developed fixes.

2002 Top Semiconductor Equipment Suppliers

Company	Website	Revenues ($M)
Applied Materials (AMAT)	www.appliedmaterials.com	5,100
Tokyo Electron Ltd. (TOELF.PK)	www.telusa.com	2,650
ASML (ASML)	www.asml.com	1,875
KLA-Tencor (KLAC)	www.kla-tencor.com	1,420
Nikon (NINOF.PK)	www.nikon.com	1,100
Canon (CAJ)	www.canon.com	850
Novellus (NVLS)	www.novellus.com	840
Dainippon Screen (DINRF.PK)	www.screen.co.jp/index.html	740
Lam Research (LRCX)	www.lamrc.com	730
Hitachi High-Technologies (8036.T)	www.hitachi-hitec.com/oversea	630
ASM International (ASMI)	www.asm.com	560
Varian Semiconductor Equipment (VSEA)	www.vsea.com	335
Veeco Instruments (VECO)*	www.veeco.com	230

*See "*Building the FC*," July 2002.

Go to www.DPRreferences.com for direct links to the indicated URLs and/or additional reference information.

Applied builds a wide array of additional tools that are required to make the main photolithography, deposition, and etching tools work properly. Wafers have to be very precisely and delicately polished between processing stages, for example, to maintain perfectly planar surfaces on which the next layer of material gets deposited. Chemical mechanical planarization (CMP) tools perform that function. Applied was a late arrival when it got into the CMP business several years ago; today, it provides about half of all CMP tools.

The company is now headed toward capturing a similar share of the cleaning tool business—currently a $1.5-billion market worldwide. No current provider dominates in the provision of wafer-cleaning tools; instead, a number of smaller companies provide legacy technologies. Small wonder, perhaps: cleaning sounds even more mundane than polishing. Yet cleaning is an essential step between each successive stage of building, and the smaller the structures get, the more finely the cleaners must scrub—contaminants that rank as mere pebbles on the highway in larger-line processes can look like boulders on smaller lines. Cleaning machines have to remove chemicals, photoresist, and contaminants; they require chemical baths with scrub brushes, ultrasonic machines, vapor and plasma dryers, and even more to remove sub-micron particles.

Last year, Applied began selling its "Oasis Clean" tool optimized for smaller contaminants and 300 mm wafers. Oasis Clean uses a combination of spin-on chemical cleaning and very high frequency ultrasonic ("megasonic") agitation. Much as the photolithographers require higher frequency light to print finer lines,

the cleaners require higher frequency sound (800 to 1000 kHz) to shake loose smaller nanometer-scale particles. Applied's unique chemical formulation (developed in a joint venture with Mitsubishi Chemical (MCMMF.PK)) has the additional advantage of removing particles, organics, and metals in a one-step process; traditional methods involve two separate steps. As a result, Applied's high throughput tool (200 wafers/hour) occupies one-third the floor space.

A chip fab requires many other large, highly specialized tools, each one a product of fantastically elaborate engineering, each one designed to engineer fantastically delicate structures a hundred million times smaller. And most of them will have to be replaced entirely in the course of the perfect-storm retooling. Ion implantation tools, for example, use beams of ions to "dope" the silicon—depositing material below, rather than on top of, the silicon surface. Applied's Quantum II ion implanter, announced last year, has been designed specifically for the sub-100 nm chip fab; it delivers higher beam currents and greater precision.

Test equipment is essential, too, at every stage of the processing. Test equipment's share of fab capital spending is expected to double for the small geometries on 300 mm wafers. Applied has a hand in this business as well, specifically for some of the critical in-line metrology. Applied's world-class NanoSEM 3D system is the industry's first critical-dimension scanning electron microscope capable of meeting the metrology challenges of sub-50 nm chip manufacturing and is functional all the way down to 20 nm gates. The "3D" refers to the broad range of multidirectional electron beam tilt angles that provide views of both the top and sides of structures—a marked improvement over conventional top-view CD metrology tools.

All in all, the diversity, complexity, and precision of chip-fab tools has no analog in any other industry. Car manufacturers assemble five thousand discrete components; jumbo aircraft production lines assemble one million; the microprocessor chip fabs assemble hundreds of millions today and will hit hundreds of billion before too much longer. Industrial robots, including the pick-and-place machines that assemble circuit boards, handle components as small as a millimeter or so in size; the chip fabs now work at the scale of tens of nanometers, which is to say, four or five orders of magnitude smaller. And alone in the industrial world, the chip fabs manufacture 500-layer structures, in which a single mistake in any one layer renders the entire structure completely useless. The builders of high rises, aircraft, cars, and even space shuttles operate in a far more resilient and forgiving engineering environment.

For a remarkable roadmap of the electrical, chemical, mechanical, and material engineering advances on which the future of the information-technology industry depends, take a look at the *International Technology Roadmap for Semiconductors* (International SEMATECH 2002). This isn't a report about wishful thinking or far-future possibilities; it's a hard-nosed analysis of concrete, attainable objectives—attainable because the engineering processes and tools are at hand, or can be developed quite quickly. They will be, with Applied Materials leading the way.

The Trough before the Storm

Last year finally saw a modest 1.3 percent growth in total global chip sales, following the previous year's 32 percent collapse. The toolmakers still didn't see an '02 uptick; their global sales fell another 24 percent last year, pushing them down to 50 percent below their Y2K, $50-billion peak. Most chip manufacturers are still, clearly, squeezing production out of existing tools and lines—and postponing construction of 300 mm lines. (Only 6 percent of world fab capacity is on 300 mm wafers.) And when times in an industry get this bad, it's all too easy to suppose that they will be bad forever.

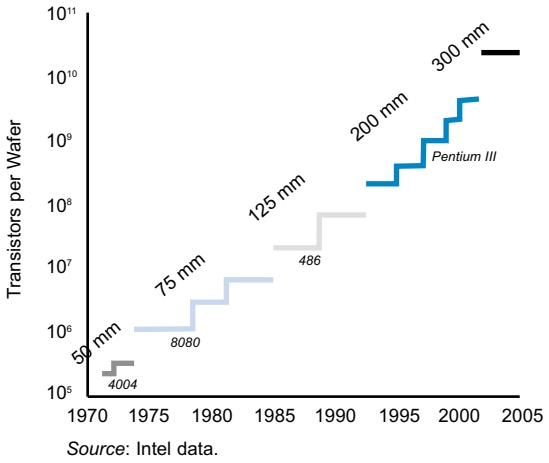
They won't. Applied hasn't stopped innovating. While investors hunker down, Applied, along with countless other smaller innovators, continues to display remarkable persistence and irrepressible ingenuity. Last month we attended a meeting that Intel convened to explore emerging technologies. Driving through Silicon Valley, we saw the abundance of empty parking lots and the profusion of "Your Name Here" signs on gleaming, empty offices. But more are still occupied, and in one of them, we had the privilege of listening in on an animated discussion of molecular mechanics, chemistry, and quantum physics between two master toolmakers. Chung Lee, CEO of private Dielectric Systems, has designed a new tool capable of building insulating layers with (by a wide margin) the lowest dielectric constant achieved so far. Ernest Demaray, formerly at Applied Materials, now CTO of the small, private Symmorphix, has produced a tool capable of building layers with the world's highest dielectric constant. (An investment firm in which we're partners recently acquired a stake in Symmorphix.) A low dielectric constant is ideal for manufacturing low-capacitance wires. A high constant is ideal for building high-capacitance capacitors. It is the classic symphony of technology—huge companies like Applied, and tiny ones like Dielectric Systems and Symmorphix, doubling and redoubling the performance of the materials, structures, and processes that define the information age.

How then can even the most dour of investors seriously imagine that the music has stopped? Can anyone seriously suppose that our economy will be unable to find uses for a billion-transistor 30 GHz chip that costs less than a Pentium? Or that the billions of people worldwide who have yet to connect to either wired or wireless networks and join the global economy will not eagerly buy hundreds of millions of 25-cent Pentiums? The 29,000-transistor 8086 microprocessor gave way to the 1.2-million-transistor 486, which gave way to the 50-million-transistor Pentium. Today we sell more of all of them, billions of 8086-equivalent chips, because they're so cheap, and hundreds of millions of Pentiums, because they're so powerful, by today's standards if not by tomorrow's. Jim Morgan was at Applied Materials in 1978 when the 8086 heralded the ascendance of the digital age, and Morgan's law has been driving the industry's economics ever since. Wafers with 3-million transistors in 1978 gave way to wafers with 30-billion transistors today, and the path to the 1-trillion-transistor wafer is now clear.

While logic and memory devices still drive most of the demand for semiconductor manufacturing tools, new horizons of demand are opening as well. Flat panel displays begin with special glass (very high tech, though still a shabby cousin of perfect silicon crystal), on which are deposited layers of amorphous silicon, silicon oxides, and silicon nitrides to make the sprawl of "thin film transistors" (TFTs) required to light the pixels in a liquid crystal display. Flat panel displays are the biggest "wafers" routinely processed today; predictably enough, Applied has emerged as the leader in the rapidly growing $5- billion equipment market that supplies the tools to build them. The company's latest plasma-enhanced CVD (PECVD) tool, introduced in January of this year, can handle 1500 mm by 1800 mm panels—over 30 times the area of a 300 mm wafer. And TFT displays are, of course, now rapidly pushing CRTs out of computing and soon out of TV markets—a combined global business of some 300 million screens sold per year.

The powerchips we've been writing about for the past three years are built with silicon-processing tools too. And these chips grow increasingly important as the power trains of cars, trucks, and trains get electrified (*Pontiacs and Powerchips*, November 2002); ultra-high-speed solid-state amplifiers are deployed by the billions to power wireless terminals and networks (*Powering RF Photons (II)*, February 2003); lasers invade the atom-moving business (*Photon Power,* June 2001); solid-state devices progressively encroach on gas-bulb lights (*Quantum Power*, May 2001); and solid-state sensors proliferate in weapons, cameras, cars, and appliances (*Infrared Imaging: Sense Out of Chaos*, January 2002).

Fig. 4. Morgan's Law



Source: Intel data.

Silicon-based micro-electro-mechanical systems (MEMS) define another potentially huge new sphere of manufacturing of chip-scale gyroscopes, accelerometers, sensors, pumps, microcoolers, and other comparable devices. MEMS have been over-hyped—this is still a very young market. But visit a real-world MEMS manufacturer—one we know personally is private Kionix, which manufactures MEMS-based gyroscopes—and you find a fab filled with Applied's tools.

So Wall Street analysts get it only partly right when they link Applied's prospects to the near-term fortunes of the largest buyers of silicon tools. Applied obviously can't prosper when Intel—by far the largest buyer of tools at $5.5 billion last year—isn't investing in new capital equipment. (The other heavy hitters in fab tool spending last year included $2.6 billion at TSMC (TSM), and just over $1 billion each at Samsung (00830.KS), IBM, ST Micro (STM), and Micron (MU).) But the rest of the story is equally compelling, when the investing does take off again, which it inevitably will.

The last major change in wafer size—from 125 mm to 200 mm—occurred just before, and we are confident it played a pivotal role in launching, the great tech boom of the 1990s. That one was a two-front storm—bigger wafers and smaller lines. It also, coincidentally, marked the beginning of the Clinton administration. Everyone from the president on down claimed credit for that one, but Jim Morgan at Applied Materials and the handful of other toolmakers deserve most of the credit. Now we're bracing for the three-front storm: a shift from 200 to 300 mm wafers, collapsing line widths, and the fundamentally new deposition tools and materials those smaller lines require. The perfect storm is at hand. That has to be excellent news for the economy as a whole, and for Applied Materials in particular.

Peter Huber, Mark Mills, March 11, 2003

The Power Panel

For an explanation of the ascendant digital power technology for each of these companies, see the indicated issue of the DPR.

FEATURED COMPANY	DPR ISSUE	OTHER PLAYERS IN THE ANALYZED SPACE*
II-VI (IIVI) www.iivi.com	1/03	Poly-Scientific (subs. Raytheon (RTN)); Umicore (Umicore Group, Belgium (ACUM.BE)
Advanced Power (APTI) www.advancedpower.com	12/00	Hitachi America (subs. HIT); Mitsubishi Semiconductor (subs. MIELY.PK); ON Semiconductor (ONNN); Philips Semiconductors (subs. PHG); Siliconix (SILI); STMicroelectronics (STM); Toshiba (TOSBF.PK)
American Superconductor (AMSC) www.amsuper.com	10/00	ABB (ABB); Intermagnetics General (IMGC); Waukesha Electric/SPX (subs. SPW)
Amkor Technology (AMKR) www.amkor.com	4/02	ChipPAC (CHPC); DPAC Technologies (DPAC)
Analog Devices (ADI) www.analog.com	8/01	Linear Technology (LLTC); Maxim Integrated (MXIM); STMicroelectronics (STM)
Analogic (ALOG) www.analogic.com	12/01	American Science & Engineering (ASE); Heimann Systems/Rheinmetall Group (subs. RNMBF.PK); InVision Technologies (INVN); L3 (LLL); Rapiscan/OSI Systems (subs. OSIS)
Applied Materials (AMAT) www.appliedmaterials.com	3/03	Novellus (NVLS); ASML (ASML)
C&D Technologies (CHP) www.cdtechno.com	7/02	East Penn (pvt.); Enersys (pvt.); Exide (EXTDQ.OB)
Coherent (COHR) www.coherentinc.com	6/01	OSRAM Opto Semiconductors/subs. Osram (Siemens, SI, sole shareholder); Rofin-Sinar (RSTI)
Cree Inc. (CREE) www.cree.com	5/01	AXT (AXTI); Nichia Corporation (pvt.); Toyoda Gosei Optoelectronics Products/Toyoda Gosei (div. 7282.BE)
Danaher Corp. (DHR) www.danaher.com	2/02	Emerson Electric (EMR); GE-Fanuc (JV GE (GE) and Fanuc Ltd. (FANUF.PK)); Mitsubishi Electric Automation/Mitsubishi Electric (div. MIELY.PK); Siemens (SI)
Emerson (EMR) www.gotoemerson.com	6/00	American Power Conversion (APCC); Marconi (MONI.L); Toshiba (TOSBF.PK)
Fairchild Semiconductor (FCS) www.fairchildsemi.com	1/01	(See Advanced Power entry.)
FLIR Systems (FLIR) www.flir.com	1/02	DRS Technologies (DRS); Raytheon Commercial Infrared/Raytheon (subs. RTN); Wescam (WSC, Canada)
Harris Corp. (HRS) www.broadcast.harris.com	9/02	AI Acrodyne (ACRO); EMCEE Broadcast Products (ECIN); Itelco (pvt.); Thales (THS.L)
Infineon (IFX) www.infineon.com	12/00	(See Advanced Power entry.)
International Rectifier (IRF) www.irf.com	4/00	(See Advanced Power entry.)
Itron (ITRI) www.itron.com	10/02	ABB (ABB); Invensys (ISYS.L); Rockwell Automation (ROK); Schlumberger Sema/Schlumberger Ltd. (SLB); Siemens (SI)
IXYS (SYXI) www.ixys.com	4/00	(See Advanced Power entry.)
Kemet Corp. (KEM) www.kemet.com	5/02	AVX Corporation/Kyocera Group (AVX); EPCOS (EPC); NEC Corporation (NIPNY); TDK Corporation (TDK); Vishay (VSH)
L-3 Communications (LLL) www.l-3com.com	12/02	DRS Technologies (DRS), Integrated Defense Technologies (IDE), and United Technologies (UTX)
Magnetek Inc. (MAG) www.magnetek.com	8/02	Ascom Energy Systems/Ascom (subs. ASCN, Switzerland); Astec/Emerson Electric (subs. EMR); Delta Electronics (2308, Taiwan); Tyco (TYC)
Maxwell Technologies (MXWL) www.maxwell.com	3/01	Cooper Electronic Technologies/Cooper Industries (div. CBE); NESS Capacitor/NESS Corp. (pvt.)
Microsemi (MSCC) www.microsemi.com	4/01	Semtech Corporation (SMTC); Zarlink Semiconductor (ZL)
Oceaneering Int'l. (OII) www.oceaneering.com	6/02	Alstom Schilling Robotics/ALSTOM (subs. ALS, France); Perry Slingsby Systems/Technip-Coflexip (subs. TKP); Stolt Offshore (SOSA); Subsea 7 (JV Halliburton (HAL) and DSND (DSNRF.PK))
Power-One (PWER) www.power-one.com	5/00	Artesyn Technologies (ATSN); Celestica (CLS); Lambda Electronics/Invensys (subs. ISYS.L); Tyco Electronics Power Systems/Tyco Electronics (div. TYC); Vicor (VICR)
Raytheon Co. (RTN) www.raytheon.com	10/01	BAE Systems (BA.L); Integrated Defense Technologies (IDE); Lockheed Martin (LMT); Northrop Grumman (NOC)
RF Micro Devices (RFMD) www.rfmd.com	2/03	Hitachi (HIT); Skyworks (SWKS); TriQuint (TQNT)
Rockwell Automation (ROK) www.rockwellautomation.com	9/01	Honeywell (HON); Invensys (ISYS.L); Mitsubishi Electric Automation/Mitsubishi Electric (div. MIELY.PK); Parker Hannifin (PH); Siemens (SI)
TRW Inc. (TRW)*** www.trw.com	1/01	Conexant (CNXT); Fujitsu (6702, Taiwan), Information & Electronic Warfare Systems/BAE Systems (div. BA.L); Northrop Grumman (NOC); RF Micro Devices (RFMD); Vitesse Semiconductor (VTSS)
Veeco Instruments (VECO)** www.veeco.com	7/02	Aixtron (AIX, Germany); Emcore (EMKR); FEI Company (FEIC); Riber (RIBE.LN); Thermo VG Semicon/Thermo Electron (subs. TMO)
Vishay Intertechnology (VSH) www.vishay.com	11/02	(See Advanced Power and Kemet entries.)
Wilson Greatbatch Technologies (GB) www.greatbatch.com	3/02	Eagle-Picher Industries (EGLP.PK); Ultralife Batteries (ULBI)

* Listed alphabetically; not a list of all public companies with similar or competing products; typically does not include private companies.
** Veeco and FEI Company announced a merger agreement on July 12, 2002; FEI will become a wholly owned subsidiary of Veeco.
*** Northrop Grumman and TRW announced a definitive merger agreement on July 1, 2002, in which NOC will acquire TRW.

Note: This table lists technologies in the Digital Power Paradigm and representative companies in the ascendant technologies. By no means are the technologies exclusive to these companies, nor does this represent a recomended portfolio. Huber and Mills may hold positions in companies discussed in this newsletter or listed on the panel, and may provide technology assessment services for firms that have interest in the companies.